## REMARKS

New Claims 12-21 are pending in this application. Old Claims 6 and 9-11 were rejected under the provisions of 35 U.S.C. 103(a).

Support for new claims 12-21 may be found throughout the specification including paragraphs 0011 through 0015 appearing on pages 5 and 6 and FIGS. 2a-2d and FIG. 4. Applicants respectfully submit that the claims are allowable over the art of record in that the art of record fails to teach or suggest the limitations of claim 1, including forming a dielectric layer on a substrate of an integrated circuit; patterning using a first photomask and etching the dielectric layer to form a trench; filling the trench in the dielectric layer with copper; polishing the copper and the dielectric to form a first planarized surface comprising a top polished surface of the copper and a top polished surface of the dielectric, the top polished surface of the copper and the trench defining a copper lower conductive metal portion of the interconnect line; depositing an aluminum layer on the first planarized surface; and patterning and etching the aluminum to define an upper conductive metal portion of the interconnect line, wherein the upper conductive metal portion is further defined so that the aluminum overlies the lower conductive metal portion.

It is noted that the Examiner has rejected old claims 6-7 and 9-11 under 35 U.S.C. §103 as unpatentable over the combination of A. McTeer, U.S. Patent No. 5,939,788 (McTeer) and K. Robinson et al., U.S. Patent No. 6,054,172 (Robinson). In accordance with the discussion presented below, applicants believe that the claims in their present form are allowable and distinguishable from the cited prior art references.

McTeer relates generally to improved methods for filling openings in silicon substrates with copper (abstract). McTeer notes the importance of barrier layers to prevent interdiffusion between Cu and silicon (3: 25-27) but notes problems created by voids generated in the damascene process (3: 25-27) and the need for barrier layers which are stable at the high temperatures required to reflow copper, such as for high aspect ratio holes (3: 55-60). In various embodiments, McTeer addresses these concerns by providing methods for filling openings in the

silicon by depositing diffusion barrier layers and wetting layers in various combinations on the inside surface of the opening. (4:7 through 6: 50).

It should be noted at the outset that McTeer doesn't teach forming an interconnect line having an upper portion comprised of one metal (such as aluminum) and a lower portion of the interconnect line comprising a different conductive metal (such as copper). Instead, McTeer teaches filling holes in dielectrics with thin barrier layers and wetting layers as discussed above. Caution should be exercized in interpreting McTeer's use of the tem copper or aluminum as modifier's for barrier or wetting layers. In such cases, such use does not indicate the constituency of the barrier layer but rather its function. For example, McTeer teaches (with reference to FIG. 14), an aluminum diffusion barrier layer 18 made up of typically titanium or titanium nitride (see text language, 22:56-60) and a copper diffusion barrier layer (see claim 26). As explained by McTeer (18:15-20) , a copper diffusion barrier layer 4 may be any metal nitride and includes tantalum nitride, titanium nitride, tungsten nitride, etc. There is no teaching or suggestion that it contains copper, but rather the opposite that it prevents diffusion of copper layers. None of these form the upper and lower conductive metal portions of the interconnect line as defined in the claims.

The examiner had also referred to McTeer and various diagrams including FIGS. 1-5 and 13 to teach some of the elements of independent claims 6 and11. As noted above, McTeer generally relates to depositing barrier layers and seed layers on the inside surfaces of contact holes. But none of the FIGS. Relied upon by the examiner in the previous rejections show a conducting line having aluminum upper portion and a copper lower portion, nor defining the aluminum upper portion of the conductor as recited in claim 12. At best McTeer teaches a vertical via with a damascene aluminum via formed over a metal plug. (10:23-44). This is neither a trench formed in the dielectric nor a structure resulting from depositing an aluminum layer on the planarized surface followed by patterning and etching of the aluminum.

McTeer either alone or in combination with Robinson, also fails to teach or suggest the claimed limitation that the same mask is used to pattern the dielectric layer and the aluminum, as in claim 13. Moreover, there is no teaching or suggestion that the mask is used in a reversed tone

to form the patterning of the aluminum. Accordingly, the art of record fails to teach or suggest all elements of claim 13.

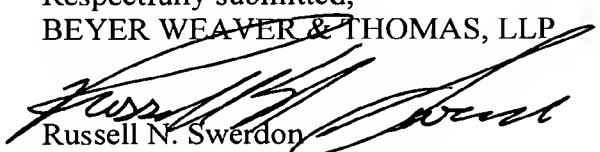
Further, as to dependant claims 21, none of the cited prior art references teaches the additional limitation "wherein the thickness of the copper and the thickness of the aluminum are adjusted so that the completed interconnect line has a first predefined electrical resistance within the range of 0.012 to 0.008 Ω per unit length." The examiner on page 5 of the office action rejected claim 10 based on McTeer 1: 39-45 and 18:60-65). But McTeer at that location only teaches forming a silicide to obtain low resistance and further teaches that the industry has migrated to investigating copper as a more conductive metal compared to aluminum. McTeer is silent as to selecting thickness of copper and aluminum and adjusting the thickness of both to meet the resistance characteristics in the ranges recited in the claims. Thus, for at least this reason, McTeer in combination with Robinson fails to teach the elements any of claims 19-21.

Dependant claims 13-21 are dependant from claim 12 ands are submitted to be allowable at least due to this dependency.

## Conclusion

Accordingly, it is submitted that all issues in the Office Action have been addressed, and withdrawal of the rejections is respectfully requested. Applicants believe that this application is in condition for allowance, and respectfully request a prompt passage to issuance. If the Examiner believes that a telephone conference would expedite the prosecution of this application, he is invited to contact the Applicants' undersigned attorney at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



Russell N. Swerdon
Registration No. 36,943

P.O. Box 778
Berkeley, CA 94704
(510) 843-6200

APPENDIX

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**(Includes All pending Claims)**

**CLAIMS**

6. (cancelled without prejudice)

9-11. (cancelled without prejudice)

12. (new) A method for fabricating a low resistance interconnect line in an integrated circuit, the method comprising the steps of:

forming a dielectric layer on a substrate of an integrated circuit,

patterning and etching the dielectric layer to form a trench, wherein the patterning is performed using a first photomask;

filling the trench in the dielectric layer with copper;

polishing the copper and the dielectric to form a first planarized surface comprising a top polished surface of the copper and a top polished surface of the dielectric, wherein the top polished surface of the copper and the trench define a lower conductive metal portion of the interconnect line, the lower conductive metal portion comprising copper;

depositing an aluminum layer on at least a portion of the top polished surface of the dielectric and at least a portion of the top polished surface of the copper of the first planarized surface; and

patterning and etching the aluminum to define an upper conductive metal portion of the interconnect line, wherein the upper conductive metal portion is further defined so that the aluminum overlies the lower conductive metal portion.

13. (new) The method for fabricating low resistance interconnect lines as recited in claim 12 wherein the first photomask is used to pattern the aluminum layer to define the upper conductive metal portion of the interconnect in a tone reversed from that used for patterning and etching the dielectric.

14. (new) The method for fabricating low resistance interconnect lines as recited in claim 12 wherein the low resistance interconnect comprises two layers of conductive metal over its length between a first connection point and a second connection point in the integrated circuit, wherein the lower conductive metal layer comprises copper and the upper conductive metal layer comprises aluminum.

15. (new) The method for fabricating low resistance interconnect lines as recited in claim 12 wherein the aluminum layer is deposited directly on the first planarized surface.

16. (new) The method for fabricating low resistance interconnect lines as recited in claim 12 further comprising depositing a barrier layer directly on the first planarized surface.

17. (new) The method for fabricating low resistance interconnect lines as recited in claim 16 wherein the aluminum layer is deposited directly on the barrier layer.

18. (new) The method for fabricating low resistance interconnect lines as recited in claim 16 wherein the barrier layer is at least one of Ta or TaN ranging from 0.005 to 0.050 μm in thickness.

19. (new) The method for fabricating low resistance interconnect lines as recited in claim 18 wherein the copper has a thickness within the range of 0.3 to 2.0 μm and the aluminum has a thickness within the range of 0.5 to 3.0 μm.

20. (new) The method for fabricating low resistance interconnect lines as recited in claim 12 wherein the copper has a thickness within the range of 0.3 to 2.0 μm and the aluminum has a thickness within the range of 0.5 to 3.0 μm.

21. (new) The method for fabricating low resistance interconnect lines as recited in claim 20 wherein the thickness of the copper and the thickness of the aluminum are adjusted so that the completed interconnect line has a first predefined electrical resistance within the range of 0.012 to 0.008 Ω per unit length.